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PC104-386L-2MB **PC/104 386SX**

CPU Module User's Manual

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- Description of you peripheral attachments
- Description of you software (operating system, version, application software, etc.) and BIOS configuration
- Description of the symptoms (Extract wording any message)

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Static Electricity Precautions

Before removing the board from its anti-static bag, read this section about static electricity precautions.

Static electricity is a constant danger to the computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always the best to safeguard against accidents, which may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system components, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the “golden finger” connectors on the bottom of every board.

Table of contents

CHAPTER 1 OVERVIEW 1
1.1 INTRODUCTION 1
1.2 SERIES COMPARISON TABLE 1
1.3 FEATURES 2
1.4 PACKING LIST 3
CHAPTER 2 SYSTEM CONTROLLERS 5
2.1 MICROPROCESSOR 5
2.2 DMA CONTROLLER 5
2.3 KEYBOARD CONTROLLER 6
2.4 INTERRUPT CONTROLLER 6
I/O Port Address Map 7
Real-Time Clock and Non-Volatile RAM 8
Timer 8
2.5 SERIAL PORTS 9
2.6 PARALLEL PORTS 11
HARDWARE FEATURES 15
2.7 BOARD OVERVIEW 15
2.8 INDEX TO JUMPERS & CONNECTORS 16
2.9 SYSTEM SETTINGS 16
Keyboard/Mouse Connector (J5) 17
PC/104 Connector (CN7 & CN8) 19
Hard Disk (IDE) Connector (CN6) 22
Reset Header (J1) 23
Parallel Port Connector (CN1) 24
Power Connector (J7) 25
Serial Ports 26
LAN Connector (J6: 6-pin 2.5mm JST) 28
CPU Base Clock Select (JP2) 29
CHAPTER 3 FLASH DISK 30
3.1 OVERVIEW 30
3.2 SWITCH SETTING 31
SSD Memory Type Select (Switch 1-1 & 1-2) 31
Programming SSD (Floppy) 32
Programming SSD (HDD) 33
D.O.C. Installation (U12) 34
SSD (Flash) Type Supported 34
CHAPTER 4 INSTALLATION 35
4.1 INSTALLATION PROCEDURES 35
4.2 CD ROM 36
BIOS FLASH Utility 36
LAN Utility 36
4.3 WATCHDOG TIMER 37
Watchdog Timer Setting 37
Watchdog Enabled/Disabled - INDEX 37H 38
Select Watchdog Report Signal - INDEX 38H 38
Timeout Status & Reset Watchdog - INDEX 3CH 39
Programming Watchdog - Basic Operation 39
4.4 PROGRAMMING RS-485 40
CHAPTER 5 BIOS SETUP 43
5.1 BIOS SETUP OVERVIEW 43
5.2 STANDARD CMOS SETUP 45
5.3 ADVANCED CMOS SETUP 47

5.4 ADVANCED CHIPSET SETUP *51*
5.5 PERIPHERAL SETUP *53*
5.6 AUTO-DETECT HARD DISKS *55*
5.7 PASSWORD SETTING *55*
Setting Password 55
Password Checking 55
5.8 LOAD DEFAULT SETTINGS *56*
Auto Configuration with Optimal Settings 56
Auto Configuration with Fail Safe Settings 57
5.9 BIOS EXIT *58*
Save Settings and Exit 58
Exit Without Saving 59
5.10 BIOS UPDATE *60*
APPENDIX 61
SPECIFICATIONS *61*
PLACEMENT *62*
DIMENSIONS *63*

List of Figures

Figure 2-1 Printer Status Buffer 12
Figure 2-2 Printer Control Bit Definitions 13
Figure 3-1 System Components Overview 15
Figure 3-2 J5: 6-Pin JST Keyboard Connector 17
Figure 3-3 CN2: Floppy Connector 18
Figure 3-4 CN8: 64-Pin PC/104 Connector Bus A & B 19
Figure 3-5 CN7: 40-Pin PC/104 Connector Bus C & D 20
Figure 3-6 CN6: Hard Disk (IDE) Connector 22
Figure 3-7 J1: Reset Header 23
Figure 3-8 CN1: Parallel Port Connectors 24
Figure 3-9 Power Connectors 25
Figure 3-10 RS-232 Connector 26
Figure 3-11 RS-485 Connector 27
Figure 3-12 LAN/RJ45 Connector 28
Figure 3-13 JP2: CPU Base Clock Select 29
Figure 4-1 DOC/FLASH Setting 31
Figure 5-1 Watchdog Block Diagram 37
Figure 6-1 BIOS Main Menu 44
Figure 6-2 Standard CMOS Setup 45
Figure 6-3 Advanced CMOS Setup 47
Figure 6-4 Advanced Chipset Setup 51
Figure 6-5 Peripheral Setup 53
Figure 6-6 Enter New Super User Password 55
Figure 6-7 Load High Performance Setting 56
Figure 6-8 Load Failsafe Setting 57
Figure 6-9 Save Current Settings and Exit 58
Figure 6-10 Quit Without Saving 59

List of Tables

Table 2-1 DMA Channel Controller 5
Table 2-2 Interrupt Controller 6
Table 2-3 I/O Port Address Map 7
Table 2-4 Real-Time Clock & Non-Volatile RAM 8
Table 2-5 ACE Accessible Registers 9
Table 2-6 Serial Port Divisor Latch 11
Table 2-7 Registers' Address 11
Table 3-1 J1 Pin Assignments 17
Table 3-2 Floppy Connector Pin Assignments 18
Table 3-3 CN8: 64-Pin PC/104 Connector Bus A & B 19
Table 3-4 CN7: 40-Pin PC/104 Connector Bus C & D 20
Table 3-5 PC/104 ISA Pin Assignments 21
Table 3-6 CN6: Hard Disk (IDE) Connector 22
Table 3-7 Parallel Port Pin Assignments 24
Table 3-8 RJ-45 Pin Assignments 28

CHAPTER 1 OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The PC104-386L-2M is a mature and well-developed PC/104 size 386SX module. It provides much greater performance such as support for onboard 2MB DRAM, two RS-232C/485 port, 1 parallel ports and 3 socket for flash disk or 1 socket for DiskOnChip® with up to 288 MB memory capacity.

The PC104-386L-2M also comes with a programmable Watchdog timer and other typical interfaces. It is excellent for embedded systems, MMI's, workstations, medical applications or POS/POI systems. As well, an RS-232C/485 port provides the remote control.

1.2 SERIES COMPARISON TABLE

Model	PC104-386L-4M	PC104-386-4M
Processor	ALI6117C	ALI6117C
Chipset	ALI6117C	ALI6117C
BIOS	AMI	AMI
DRAM	2MB(4MB Max.)	2MB(4MB Max.)
Watchdog Timer	Yes	Yes
Multi I/O Chip	One	One
SSD Interface	FLASH/DOC	FLASH/DOC
IDE/FDD	Yes	Yes
2S/1P(RS232/RS485)	Yes	Yes
Ethernet 10Mbps	One	No
Board Size	185mm x 122mm	185mm x 122mm

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- Up to 40 MHz 386SX single board computer.
- Stack through PC/104 expansion bus.
- 2 MB EDO RAM on-board & 2 MB space for expansion.
- 10Base-T NE2000 compatible network. (Without on FB2310A)
- Parallel port, floppy and IDE Interface.
- 2 RS-232C/RS-485 serial ports. (RS-485 is optional)
- PS/2 compatible keyboard interface.
- E2KEY function for safe CMOS data keeping. (Option)
- On-board LED indicator and speaker header.
- Flash BIOS with easy upgrade utility.
- Software programmable watchdog timer.
- 3 sockets for 1.5MB flash disk or - 2 sockets for 1MB flash disk and 1DIP socket for up to 288 MB DiskOnChip.
- Low power consumption, +5V only, 1.2A maximum.
- EMI Considered on every output signals.
- PC/104 form factor, 90.2 mm x 95.9 mm. (3.55” x 3.775”)

1.4 PACKING LIST

The following accessories are included in the package. Before you begin installing your PC104-386L-2M board, take a moment to make sure that they have been included inside the PC104-386L-2M package.

- 1 PC104-386L-2M all-in-one CPU board.
- 1 44-pin hard disk drive interface cable.
- 1 20-pin to 34-pin floppy drive interface cable.
- 1 parallel port interface cable.
- 2 serial port adapter cables. (10-pin IDC to DB-9)
- 1 LAN adapter cable. (JST to RJ45) Without FB2310A
- 1 PS/2 keyboard adapter cable.
- 1 power adapter cable.
- 1 CD includes necessary utility drivers, quick setting guide file, and this manual file
- A hard copy of User's quick setting guide

NOTE: *If any of the listed accessories is missing or damaged, please contact your dealer for immediate servicing.*

CHAPTER 2 SYSTEM CONTROLLERS

This chapter describes the major structure of the PC104-386L-2M CPU board. The following topics are covered:

- Microprocessor
- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Serial Ports
- Parallel Ports

2.1 MICROPROCESSOR

The PC104-386L-2M uses the ALI M6117 CPU; it is designed to perform systems like Intel's 386SX system with deep green features.

The 386SX core is the same as M1386SX of Acer Labs. Inc. and 100% object code compatible with the Intel 386SX microprocessor. System manufacturers can provide 386 CPU based systems optimized for both cost and size. Instruction pipelining and high bus bandwidth ensure short average instruction execution time and high system throughput. Furthermore, it can keep the state internally from charge leakage while external clock to the core is stopped without storing the data in registers. The power consumption here is almost zero until the clock stops. The internal structure of this core is 32-bit data and address bus with very low supply current. Real mode as well as Protected mode are available and can run MS-DOS /MS-Windows.

2.2 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the PC104-386L-2M board.Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.3 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The "output buffer full" interruption may be used for both send-and-receive routines.

2.4 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the PC104-386L-2M board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

The following table contains the system information of hardware interrupt priorities:

System Interrupt	IRQ	Function	Priority
08h	IRQ 0	System timer (Timer Channel 0 output)	1
09h	IRQ1	Keyboard controller output buffer full interrupt	2
0Ah	IRQ 2	Cascade from second programmable interrupt	-
0Bh	IRQ 3	COM2	10
0Ch	IRQ 4	COM1	11
0Dh	IRQ 5	Parallel port 2	12
0Eh	IRQ 6	Floppy diskette adapter	13
0Fh	IRQ 7	Parallel port 1	14
70h	IRQ 8	Real Time Cock	15
71h	IRQ 9	COM4	3
72h	IRQ 10	LAN adapter	4
73h	IRQ 11	COM3	5
74h	IRQ 12	Reserved for PS/2 mouse	6
75h	IRQ 13	Math coprocessor	7
76h	IRQ 14	Hard diskette adapter	8
77h	IRQ 15	Reserved for Watchdog	9

Table 2-2 Interrupt Controller

I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	ALI M6117 chipset address
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-3 I/O Port Address Map

Real-Time Clock and Non-Volatile RAM

The PC104-386L-2M contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-4 Real-Time Clock & Non-Volatile RAM

Timer

The PC104-386L-2M provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.Application programs can load different counts into this timer to generate various sound frequencies.

2.5 SERIAL PORTS

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

Table 2-5 ACE Accessible Registers

➲ ***Receiver Buffer Register (RBR)***

Bit 0-7: Received data byte (Read Only)

➲ ***Transmitter Holding Register (THR)***

Bit 0-7: Transmitter holding data byte (Write Only)

➲ ***Interrupt Enable Register (IER)***

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

➲ ***Interrupt Identification Register (IIR)***

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

➲ ***Line Control Register (LCR)***

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

➲ ***MODEM Control Register (MCR)***

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

➲ ***Line Status Register (LSR)***

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

➲ ***MODEM Status Register (MSR)***

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

➲ ***Divisor Latch (LS, MS)***

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-6 Serial Port Divisor Latch

2.6 PARALLEL PORTS

➲ ***Register Address***

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

Table 2-7 Registers' Address

➲ ***Printer Interface Logic***

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

➲ ***Data Swapper***

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

➲ ***Printer Status Buffer***

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

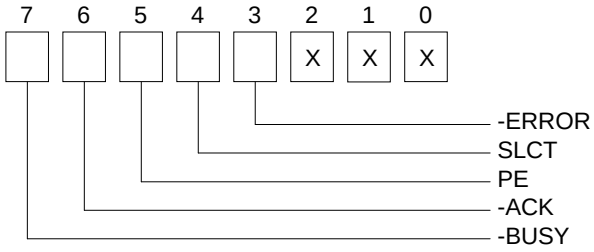


Figure 2-1 Printer Status Buffer

NOTE: *X represents not used.*

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A 1 means the printer has detected the end of the paper.

Bit 4: A 1 means the printer is selected.

Bit 3: A 0 means the printer has encountered an error condition.

➲ ***Printer Control Latch & Printer Control Swapper***

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

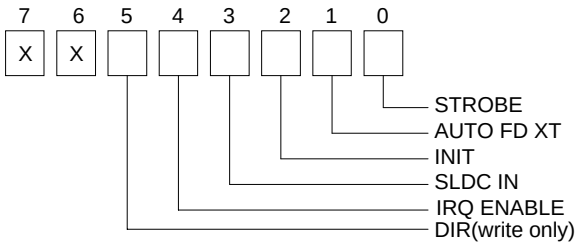


Figure 2-2 Printer Control Bit Definitions

NOTE: *X represents not used.*

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is writing only.

Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A 1 in this bit position selects the printer.

Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

HARDWARE FEATURES

This section describes the pin assignments for system's external connectors and the jumper settings.

- Board Overview
- System Setting

2.7 BOARD OVERVIEW

The PC104-386L-2M is a PC/104 386SX CPU module. This section provides hardware jumper settings, the connectors' locations, and the pin assignment.

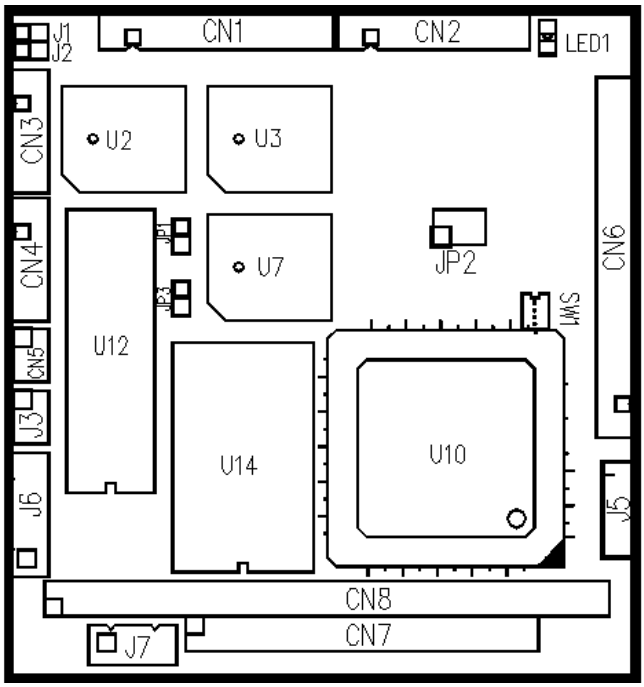


Figure 0-1 System Components Overview

2.8 INDEX TO JUMPERS & CONNECTORS

The following lists the jumper and connector functions for reference.

Label	Function
J1	2 pin reset header
J2	Header External Speaker
J3	External LED
J5	Keyboard Connector (6 pin 2.0 mm JST)
J6	External RJ45 connector
J7	Power Connector (4 pin 2.0 mm JST)
JP1/JP3	3-pin COM1/COM2 RS485 terminator
JP2	CPU base clock select
CN1	26-pin parallel ports
CN2	20-pin floppy connector
CN3	COM1-RS232 connector
CN4	COM2-RS232 connector
CN5	6-pin RS-485 connector
CN6	44-pin hard disk connector
CN7	40-pin PC/104 connector C&D
CN8	64-pin PC/104 connector Bus A&B
U2, U3, U12	Socket for flash and DOC.
SW1	D.O.C./SRAM select

2.9 SYSTEM SETTINGS

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the PC104-386L-2M jumper pins, and the factory-default settings.

CAUTION: *Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage the electronic components.*

Keyboard/Mouse Connector (J5)

6-Pin JST Keyboard/Mouse Connector (J5)

The following demonstrates the pin assignments of the 6-pin JST keyboard/mouse connector. To use the PS/2 mouse, an optional adapter cable has to be connected to the J5 (6-pin header type) connector. The pin assignments for the JST connector are as follows

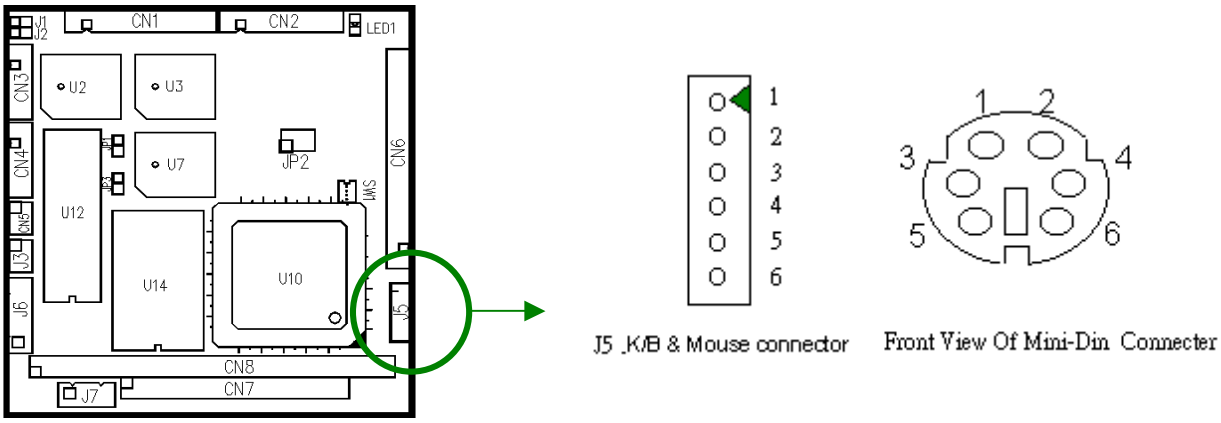


Figure 0-2 J5: 6-Pin JST Keyboard Connector

Pin	Signal
1	Mouse Data
2	Keyboard Data
3	Ground
4	VCC
5	Mouse Clock
6	Keyboard Clock

Table 0-1 J1 Pin Assignments

Floppy Connector (CN2: 20-pin 2.0mm IDC)

The included floppy drive interface cable is used to transfer 20-pin connector into standard 34-pin connector. The following table shows signal connections between 20-pin & 34-pin connectors.

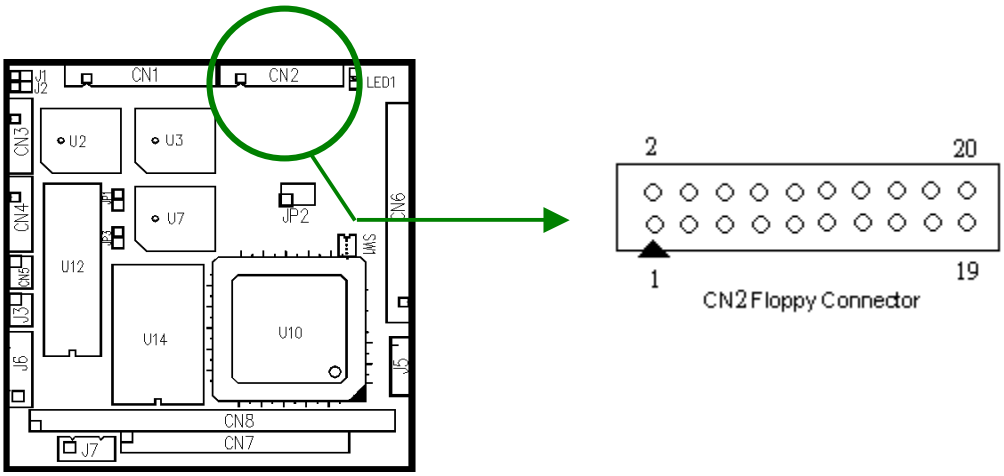


Figure 0-3 CN2: Floppy Connector

20-pin	Signal	34-pin	20-pin	Signal	34-pin
1	Drive Enable A	2	11	-Write Data	22
2	-Index	8	12	Ground	23
3	-Select A	12	13	-Write Enable	24
4	Ground	11	14	-Track 0	26
5	-Motor A	16	15	-Write Protect	28
6	- Select B	14	16	Ground	29
7	-Motor B	10	17	-Read Data	30
8	Ground	9	18	-Head	32
9	-Direction	18	19	-Disk Change	34
10	-Step	20	20	Ground	31
-	-	-	-	No Connection	Others

Table 0-2 Floppy Connector Pin Assignments

PC/104 Connector (CN7 & CN8)

(1) 64 Pin PC/104 Connector Bus A & B (CN8)

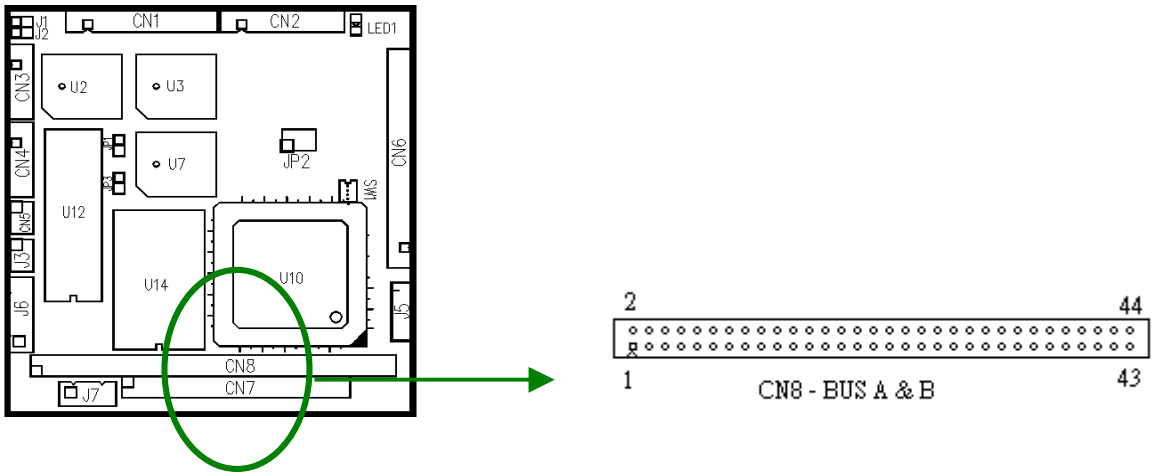


Figure 0-4 CN8: 64-Pin PC/104 Connector Bus A & B

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	-IOCHK	33	SA14	2	Ground	34	-DACK1
3	SD7	35	SA13	4	RSTDRV	36	DRQ1
5	SD6	37	SA12	6	+5V	38	-REFSH
7	SD5	39	SA11	8	IRQ9	40	BUSCLK
9	SD4	41	SA10	10	-5V (*1)	42	IRQ7
11	SD3	43	SA9	12	DRQ2	44	IRQ6
13	SD2	45	SA8	14	-12V (*1)	46	IRQ5
15	SD1	47	SA7	16	-ZWS	48	IRQ4
17	SD0	49	SA6	18	+12V	50	IRQ3
19	IORDY	51	SA5	20	Key1	52	-DACK2
21	AEN	53	SA4	22	-MEMW	54	TC
23	SA19	55	SA3	24	-MEMR	56	ALE
25	SA18	57	SA2	26	-IOW	58	+5V
27	SA17	59	SA1	28	-IOR	60	OSC
29	SA16	61	SA0	30	-DACK3	62	Ground
31	SA15	63	Ground	32	DRQ3	64	Ground

Table 0-3 CN8: 64-Pin PC/104 Connector Bus A & B

NOTE: Power input, +5V, -5V, +12V, or –12V for Pin 10 & Pin14 is supplied from the system power connected to the power connector.

(2) 40 Pin PC/104 Connector Bus C & D (CN7)

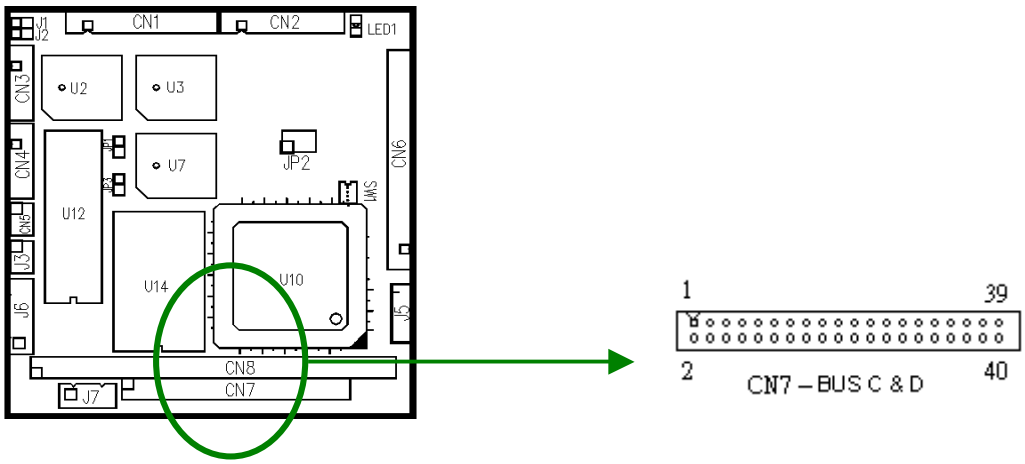


Figure 0-5 CN7: 40-Pin PC/104 Connector Bus C & D

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	21	MEMWR16	2	Ground	22	-DACK5
3	-SBHE	23	SD8	4	-MEM16	24	DRQ5
5	LA23	25	SD9	6	-IO16	26	-DACK6
7	LA22	27	SD10	8	IRQ10	28	DRQ6
9	LA21	29	SD11	10	IRQ11	30	-DACK7
11	LA20	31	SD12	12	IRQ12	32	DRQ7
13	LA19	33	SD13	14	IRQ15	34	+5V
15	LA18	35	SD14	16	IRQ14	36	-MASTER
17	LA17	37	SD15	18	-DACK0	38	Ground
19	MEMRD16	39	Key2	20	DRQ0	40	Ground

Table 0-4 CN7: 40-Pin PC/104 Connector Bus C & D

(3) PC/104 (ISA) Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0-SA19 [Input/ Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17-LA23[Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
ALE [Output]	The Buffered Address Latch Enable is used to latch SA0 – SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IORDY[Input,Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence: (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1mega bytes of memory are being used
-MEMR16 [Input/Output]	The Memory Read signal is low while any memory location is being read
-MEMW [Output]	The System Memory Write is low while any of the low 1mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFSH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
-SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEM16[Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IO16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 0-5 PC/104 ISA Pin Assignments

Hard Disk (IDE) Connector (CN6)

A 44-pin header type connector (CN6) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 44-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use BIOS Setup program to select. The following table illustrates the pin assignments of the hard disk drive's 44-pin connector.

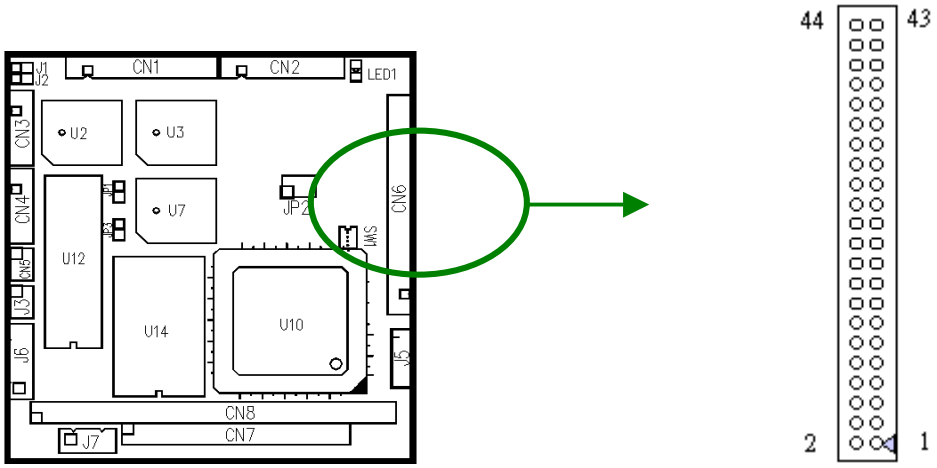


Figure 0-6 CN6: Hard Disk (IDE) Connector

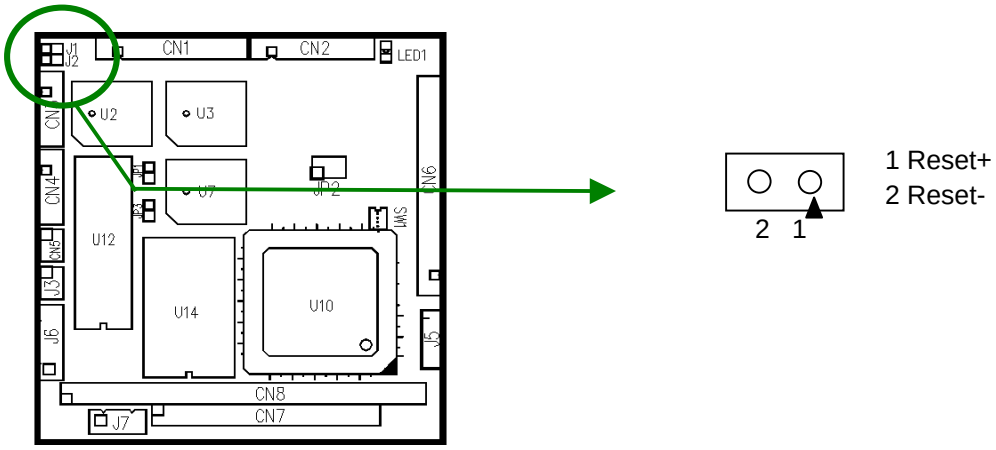
Pin	Signal	Pin	Signal
1	-RESET	2	Ground
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	Ground	20	Ground
21	Not Used	22	Ground
23	-IOW A	24	Ground
25	-IOR A	26	Ground
27	-CHRDY A	28	DALE
29	Not Used	30	Ground
31	-IRQ 14	32	-IO16
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	Ground
41	VCC	42	VCC
43	Ground	44	Not Used

Table 0-6 CN6: Hard Disk (IDE) Connector

Reset Header (J1)

J1 is used to connect to an external reset switch. Shorting these two pins will reset the system.

Figure 0-7 J1: Reset Header



Parallel Port Connector (CN1)

Use the included adapter cable to connect the 26-pin header type CN1 connector. This adapter cable is mounted on a bracket and is included in your FB2310 package. The connector for the parallel port is a 25 pin D-type female connector. The following table shows signal connections between 26-pin & DB25 connectors.

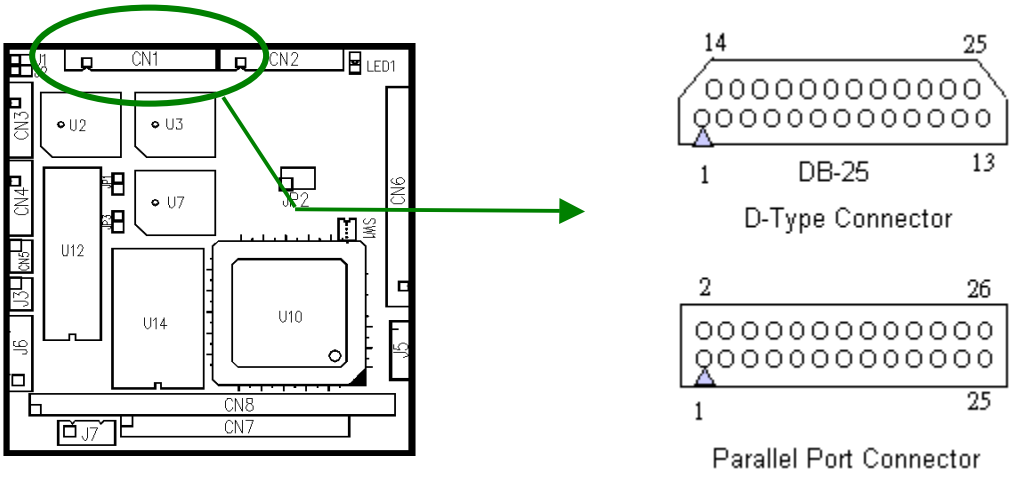


Figure 0-8 CN1: Parallel Port Connectors

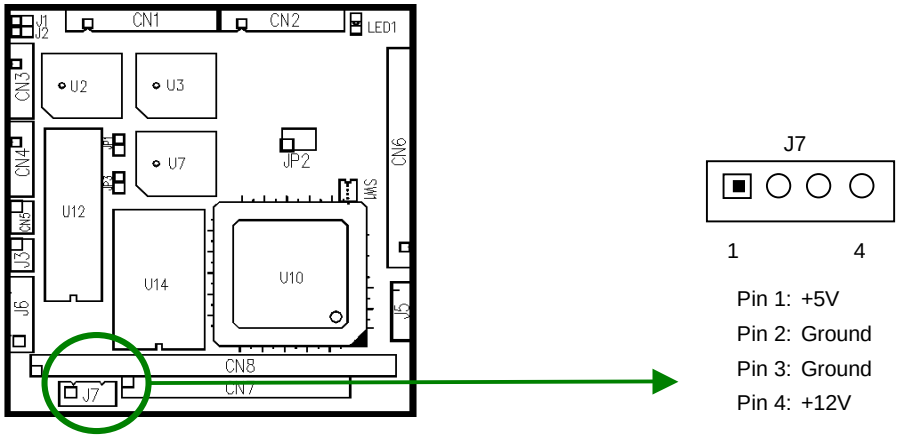
CN1	DB-25	Signal	CN1	DB-25	Signal
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

Table 0-7 Parallel Port Pin Assignments

Power Connector (J7)

J7 is a 4-pin power connector. Using the J7, you can connect the power supply to the on board power connector for stand alone applications directly.

Figure 0-9 Power Connectors



Serial Ports

A. Serial Port Connectors & Jumpers

(1) RS-232C Pin Definitions (CN3 & CN4: 10-pin 2.0mm IDC)

The included serial port adapter cables are used to transfer 10-pin IDC connector into standard DB9 connector. The following table shows signal connections of the adapter cable:

The following figure and table guide you how to set up RS-232 serial port.

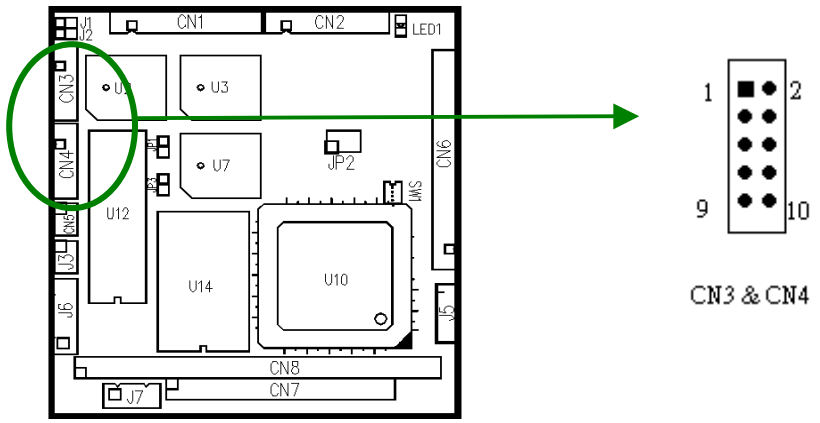


Figure 0-10 RS-232 Connector

CN3 (COM1)	Signal	DB9	CN4 (COM2)	Signal	DB9
1	-DCD1	1	1	-DCD2	1
2	-DSR1	2	2	-DSR2	6
3	RXD1	3	3	RXD2	2
4	-RTS1	4	4	-RTS2	7
5	TXD1	5	5	TXD2	3
6	-CTS1	6	6	-CTS2	8
7	-DTR1	7	7	-DTR2	4
8	-RI1	8	8	-RI2	9
9	Ground	9	9	Ground	5
10	Case Ground	-	10	Case Ground	-

Table 3-8 RS-232 Serial Port Pin Assignment

The on-board two serial ports can be configured as RS-485 mode by selecting SW1-3 and SW-4. CN5 is the RS-485 connector; JP1 and JP3 is the terminator jumper of COM1 and COM2 respectively.

SW1-3	COM1	SW1-4	COM2
Off	RS-232C	Off	RS-232C
On	RS-485	On	RS-485

Table 0-9 Serial Port RS-485 COM 1 & COM 2 Switcher

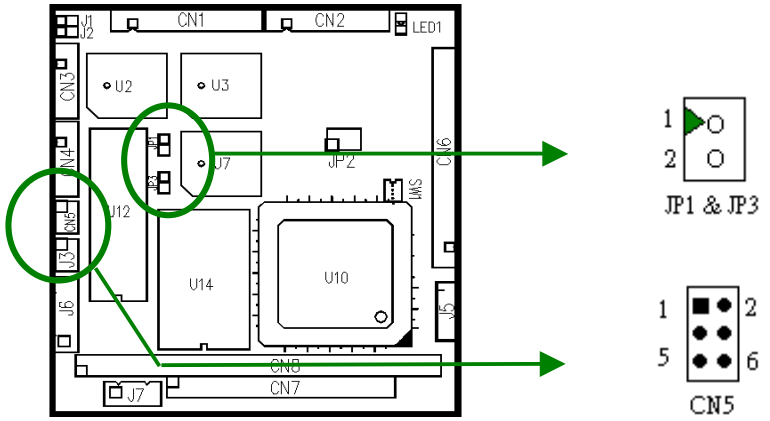


Figure 0-11 RS-485 Connector

CN5	Signal	CN5	Signal
1	485C1+	4	485C2+
2	485C1-	5	485C2-
3	Case Ground	6	Case Ground

Table 0-10 Serial Port RS-485 COM 1 & COM 2

LAN Connector (J6: 6-pin 2.5mm JST)

J6 contains LAN twist pair signals and LAN access indicator signal. The included LAN adapter cable is use to transfer to standard RJ45 connector.

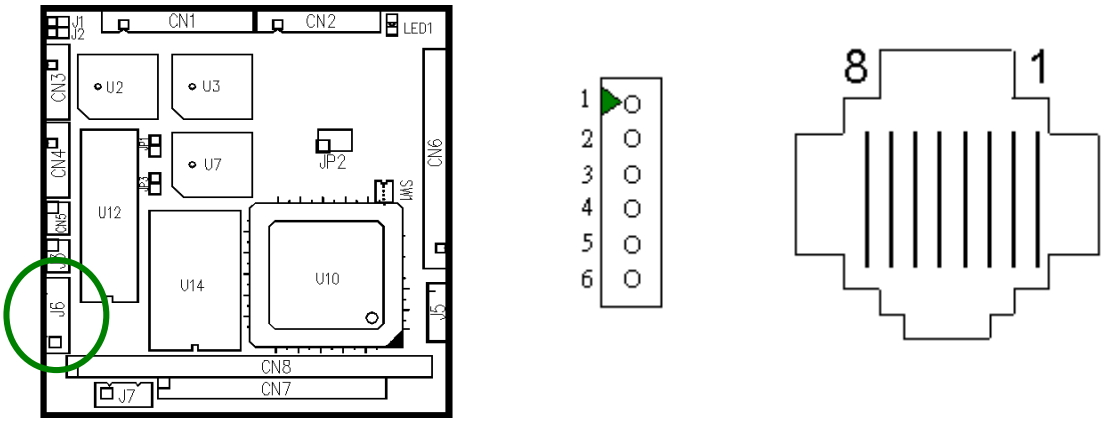


Figure 0-12 LAN/RJ45 Connector

J6	Signal	RJ45	J6	Signal	RJ45
1	TPTX+	1	-	Not Used	5
2	TPTX -	2	-	Not Used	6
3	TPRX+	3	-	Not Used	7
4	TPRX -	6	-	Not Used	8
5	Access LED+	-	6	Access LED-	-

Table 0-8 RJ-45 Pin Assignments

CPU Base Clock Select (JP2)

The CPU base clock (Input clock) is twice of its operation clock.

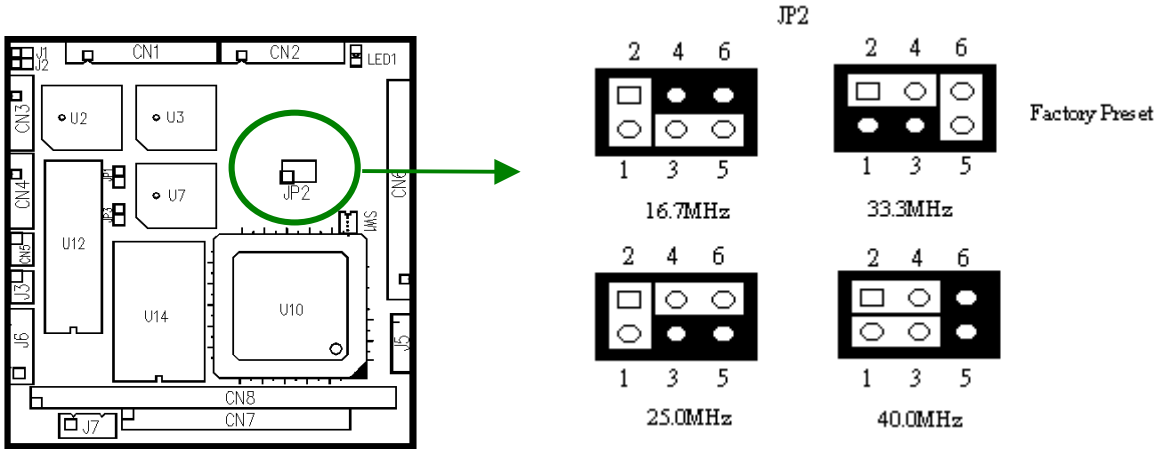


Figure 0-13 JP2: CPU Base Clock Select

CHAPTER 3 FLASH DISK

The section describes the various types of solid-state disk. The following topics are covered:

- Overview
- Switch Setting
- Programming Flash Disk
- SSD(Flash) Type Supported

3.1 OVERVIEW

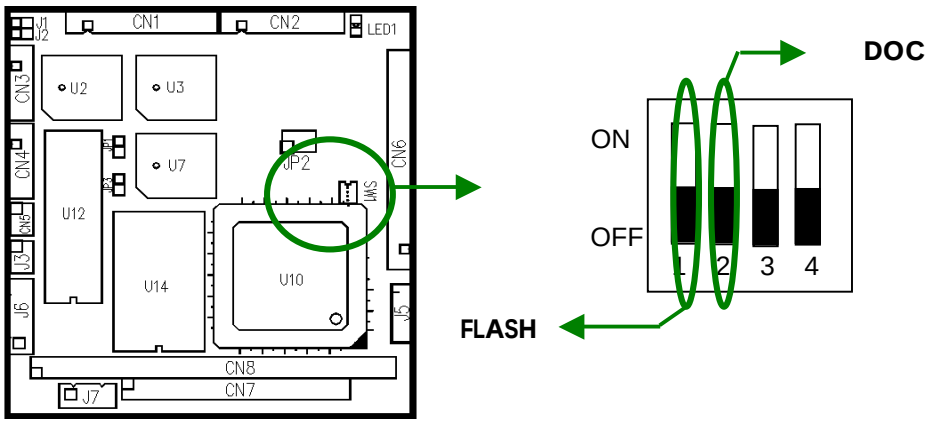
The PC104-386L-2M provides one 32-pin JEDEC DIP sockets two PLCC socket, which may be populated with up to 1.5MB/1MB of FLASH or DiskOnChip up to 288MB. It is ideal for diskless systems, high reliability and/or high-speed access applications, controller for industrial or line test instruments, and etc.

FLASH disk function enables you to use the 5V FLASH EPROM instead of UV EPROM, and allows you to directly program the FLASH disk without having to purchase any additional programming equipment. If small page (less or equal 512 bytes per page) 5V FLASHs were used, you could format FLASH disk and copy files onto FLASH disk just like using a normal floppy and hard disk. You can use all of the related DOS command (such as COPY, DEL...etc.) to update files on the 5V FLASH disk.

3.2 SWITCH SETTING

FLASH / D.O.C. DISK Select

There is a DIP Switch on the PC104-386L-2M It performs the following functions. These functions may be required to perform with relevant jumpers. Detailed settings will be specified latter.



Switch 1-1 Set the FLASH DISK mapping
Switch 1-2 Set the DOC mapping

Figure 3-1 DOC/FLASH Setting

A. Flash Disk and DOC Memory Bank Segment Settings (SW1-1 & SW1-2)

SW1-1	SW1-2	Flash Disk Memory Bank Segment	DiskOnChip Memory Bank Segment	Remark
Off	Off	C800:0 (8KBytes)	Disabled	Preset
On	Off	D800:0 (8KBytes)	Disabled	
Off	On	C800:0 (8KBytes)	CA00:0 (8KBytes)	
On	On	D800:0 (8KBytes)	DA00:0 (8KBytes)	

Note: If SSD Disk enable, the system will be reserved 32K byte

Socket	Package	Flash Disk	DiskOnChip
U2 (M1)	PLCC32	Yes	No
U3 (M2)	PLCC32	Yes	No
U12 (M3)	DIP32	Yes	Yes (If enabled)

Note: If DOC is enabled, please set SW1-2 “ON” position to enable flash function and (U12) is ready for serving DiskOnChip.

SSD Memory Type Select (Switch 1-1 & 1-2)

The Switch 1-1 & 1-2 is used to select the memory bank segment. You must select an appropriate memory bank segment so that the FB2310 will not conflict with memory installed on other add-on memory cards. Additionally, be sure not to use shadow RAM area or EMM driver’s page frame in this area.

If you are not going to use the Solid State Disk (SSD), you can use BIOS setup program to disable the SSD BIOS. The PC104-386L-2M will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page, which is used by PC104-386L-2M For

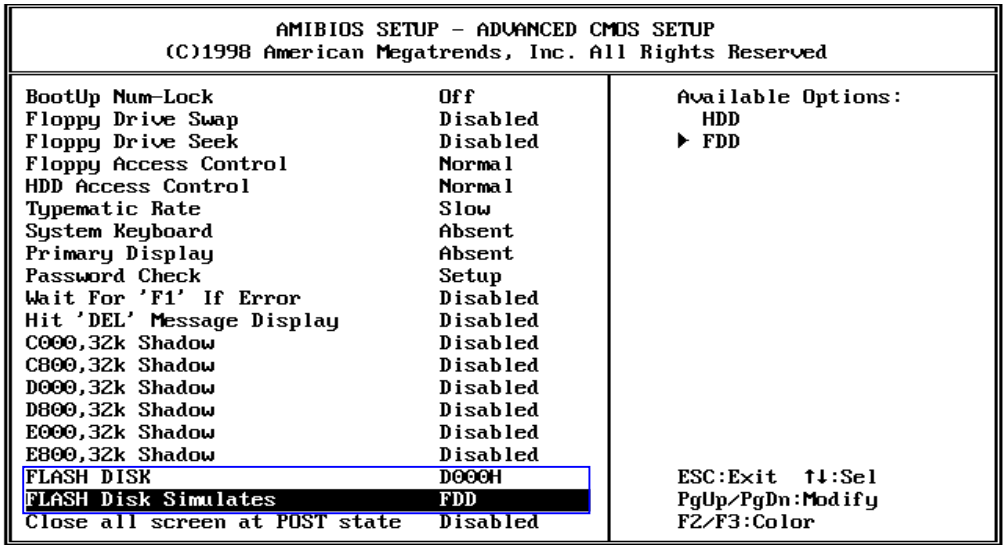
example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of PC104-386L-2M is C800:0)

DEVICE=C:\DOS\EMM386.EXE X=C800-C9FF

The sample procedure is step by step for SSD is below:

Programming SSD (Floppy)

1. Install the flash in Socket U2, U3, and U12. (Like 29C040A)
2. Set the SW1-1 to off position (The SSD data bank is C800:0)
3. Connect power to the system.
4. Power ON.
5. Press Delete key to display the BIOS Setup menu.
6. Enter CMOS Setup menu. Then choice to CMOS SET UP >ADVANCE CMOS SETUP >SSD FUNCTION set to D000H SEGMENT
7. In the Flash Disk Simulates field, select FDD that the flash disk will act as a physical floppy. Then, save the setting. (The system will be restart) the screen like below:



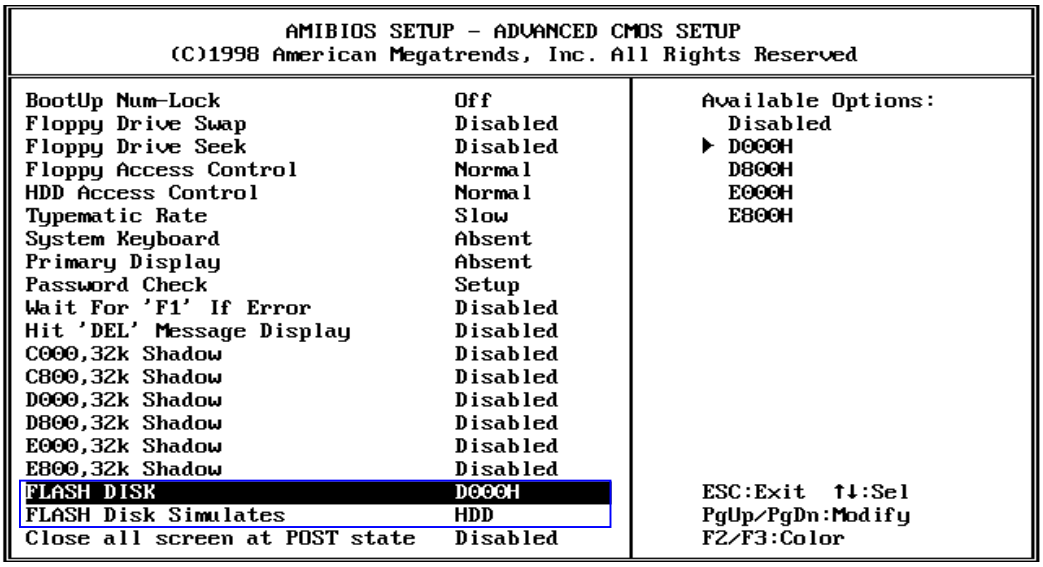
8. Press, hold down ctrl_ keys (ctrl & underline) to display the SSD Setup menu.
9. On the screen, use the up or down arrow keys to select a flash type and size. The screen like below:

PC104-386L-2M SSD BIOS version 1.20 (c) 2000 NAGASAKI Corp
Flash Disk Setting : Disk B: Unknow ??? ..1536K Maximum
Base Port Address : 0078h Firmware Seg.: D000h Data Bank Seg.: C800h
DOS Booting Driver : As BIOS Setting M4(U5) Socket Setting: SSD
ESC: Exit F5: Save & Exit ←→: Select ↓ ↑: Modify
Hit<Ctrl, _> to setup Flash disk

10. Press “F5” to save the setting. The message “Write to FLASH disk (y/n)” displayed.
11. Press “Y” key to write the setting to the Flash disk.
12. The booting from other device. (Like physical HDD or FDD)
13. Use the FORMAT command to format the flash disk in DOS mode. (This time this SSD is B:)
14. Use FORMAT B:/S /C/ U (The S: SYSTEM BOOTING /C: Check /U: UNFORMAT
If format parameter no " /S " the SSD will be always to device B: that can't boo up the system.

Programming SSD (HDD)

1. Install the flash disk in Socket U2, U3, and U12. (Like 29C040A)
2. Set the SW1-1 to off position (The SSD data bank is C800:0)
3. Connect power to the system.
4. Power ON.
5. Press Delete key to display the BIOS Setup menu.
6. Enter the CMOS Setup menu. Then choice to CMOS SET UP >ADVANCE CMOS SETUP SSD FUNCTION set to D000H SEGMENT
7. In the Flash Disk Simulates field, select HDD that the flash disk will act as a physical hard disk. Then, save the setting. The screen like below:



8. Press hold down ctrl_ keys (ctrl & underline) to display the SSD Setup menu.
9. On the screen, use the up or down arrow keys to select a flash type and size. The screen like below:

PC104-386L-2M SSD BIOS version 1.20 (c) 2000 NAGASAKI Corp
Flash Disk Setting : Disk #80h (C:) Unknow ??? ..1536K Maximum
Base Port Address: 0078h Firmware Seg.: D000h Data Bank Seg.: C800h
DOS Booting Driver : As BIOS Setting M4(U5) Socket Setting: SSD
ESC: Exit F5: Save & Exit ←→: Select ↓ ↑: Modify
Hit<Ctrl,_> to setup Flash disk

10. Press "F5" to save the setting. The message "Write to FLASH disk (y/n)" displayed.
11. Press "Y" key to write the setting to the Flash disk.
12. The booting from other device. (Like physical HDD or FDD)
13. Use the FDISK command to partition the flash disk in DOS mode. (If system is not physical HDD the SSD is C:)
14. Use FORMAT C:/S /C/ U (The S: SYSTEM BOOTING /C: Check /U: UNFORMAT
If format parameter no " /S " the SSD will be can't boot up the system.

Note: If Flash Disk Simulates field select HDD, The flash disk total size must be above to 512KB.

CAUTION: It is not recommended that the user format the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle lifetime is about 10,000 or 100,000 times, writing data to the FLASH too often will reduce the lifetime of the FLASH EPROM chips,

D.O.C. Installation (U12)

Step 1: Insert programmed DiskOnChip into sockets U12 setting as DOC.

Step 2: Adjust SW1-2 to ON.

Step 3: Line up and insert the FB2310 card into any free space of your computer.

Step 4: Use the D.O.C. in no HDD equipment, and after installed D.O.C. we can easily boot the system from D.O.C.

SSD (Flash) Type Supported

The following list contains 5V FLASHs supported by the PC104-386L-2M :

SST	PH29EE010	(128KX8, 1M bits)
SST	PH28SF040	(512KX8, 1M bits)
SST	PH28SF040A	(512KX8, 1M bits)
WINBOND	W29EE011	(128KX8, 1M bits)
ATMEL	AT29C020	
ATMEL	AT29C040	(256KX8, 2M bits)
ATMEL	AT29C040A	(512KX8, 4M bits)

CHAPTER 4 INSTALLATION

This chapter provides information for you to set up a working system based on the PC104-386L-2M CPU board. Carefully read the details of the CPU board's hardware descriptions before installation, especially the jumper settings, switch settings and cable connections. The following topics are covered:

- Overview
- CD ROM
- Watchdog Timer

4.1 INSTALLATION PROCEDURES

Follow the steps listed below to install the PC104-386L-2M system.

Step 1: Read the CPU board's hardware description in this manual.

Step 2: Set the jumpers.

Step 3: Make sure that the power supply connected to your passive CPU board is turned off.

Step 4: Connect all necessary cables. Make sure that the FDC, HDC; serial and parallel cables are connected to pin 1 of the related connector.

Step 5: Connect the hard disk/floppy disk flat cables from the CPU board to the drives. Connect a power source to each drive.

Step 6: Plug the keyboard into the keyboard connector.

Step 7: Turn on the power.

Step 8: Configure your system with the BIOS Setup program then re-boot your system.

Step 9: If the CPU board does not work, turn off the power and read the hardware description carefully again.

Step 10: If the CPU board still does not perform properly, return the board to your dealer for immediate service.

4.2 CD ROM

PC104-386L-2M provides a CD ROM includes the manual files (a complete manual file and a quick setting guide) and the required utility files.

Follow the following description to install these utility files.

BIOS FLASH Utility

In the <UTILITY> directory, there is the AMIFLASH.COM file.

1. Use the AMIFLASH.COM program to update the BIOS setting.
2. And then refer to the chapter "BIOS Setup", as the steps to modify BIOS.
3. Now the CPU board's BIOS loaded with is the newest program; user can use it to modify BIOS function in the future, when the BIOS add some functions.

LAN Utility

Step 1: To install the LAN utility, insert the CD ROM into the CD ROM device, and enter DRIVER>FB2310>LAN>UM9008. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.

Step 2 Execute install.exe file.

4.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.

The PC104-386L-2M is equipped with a programmable time-out period watchdog timer. User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system or trigger an IRQ signal. The time-out period can be programmed to be 30.5 μseconds to 512 seconds.

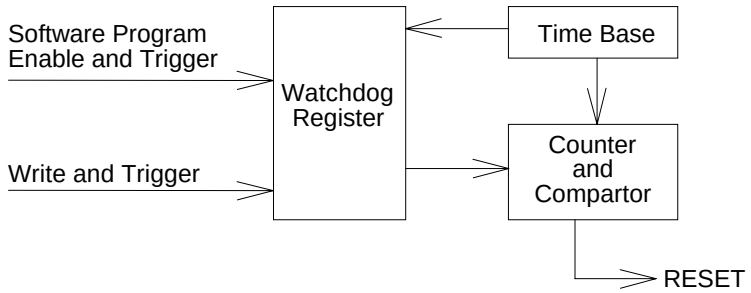


Figure 4-1 Watchdog Block Diagram

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger an IRQ signal to tell your program that the watchdog is times out.

Watchdog timer -INDEX 39H, 3AH, and 3BH

3Bh	3Ah	39h
D7…D0	D7…D0	D7…D0
Counter [MSB …LSB]		

For example

INDEX	3Bh	3Ah	39h	
	00h	00h	01h	30.5 μsec
	--	--	02h	61 μsec
	00h	01h	00h	7.8 m sec
	00h	02h	00h	15.6 m sec
	01h	00h	00h	2 sec
	02h	00h	00h	4 sec
	FFh	FFh	FFh	512 sec

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initialize the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously; otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

Watchdog Enabled/Disabled - INDEX 37H

Bit 7 Reserved. Please do not set this bit.
In old version M6117C data sheet, this bit is counter read mode.

Bit 6 0 Disable watchdog timer
1 Enable watchdog timer

Bit 5-0 Other function.
Please do not modify these bits.

Select Watchdog Report Signal - INDEX 38H

Bit 7-4 Watchdog timer time out report signal select
0000 No output signal
0001 IRQ3 selected
0010 IRQ4 selected
0011 IRQ5 selected
0100 IRQ6 selected
0101 IRQ7 selected
0110 IRQ9 selected
0111 IRQ10 selected
1000 IRQ11 selected
1001 IRQ12 selected
1010 IRQ14 selected
1011 IRQ15 selected
1100 NMI selected
1101 System reset selected
1110 No output signal
1111 No output signal

Bit 3-0 Other function.
Please do not modify these bits.

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too. Before you configure the IRQ signals, make sure they are not conflicted with other devices, like Floppy, printer, serial ports, LAN, and PS/2 mouse, etc. Refer to Table 2-2 Interrupt Controller for IRQ reference.

2. Before you initialize the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously; otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled. If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> these two items must set to ***Primary***.

Timeout Status & Reset Watchdog - INDEX 3CH

Bit 7 0 Timer timeout not happened
1 Timer timeout happened
Read only.

Bit 5 Write this bit "1" to reset timer
The value on this bit has no meaning.

Bit 6 Other function.
Bit 4-0 Please do not modify these bits.

Programming Watchdog - Basic Operation

If we would like to access M6117C configuration register, we need to unlock register at first and lock it after finishing operation.

➲ ***Unlock Configuration Register***

```
mov    al, 013h
out    22h, al
nop
nop
mov    al, 0c5h
out    23h, al
nop
nop
```

➲ ***Lock Configuration Register***

```
mov    al, 013h
out    22h, al
nop
nop
mov    al, 000h
out    23h, al
nop
nop
```

➲ ***Read the Value at Configuration Register***

For example, read INDEX 3Ch:
Unlock configuration register

```
mov    al, 03ch
out    22h, al
nop
nop
in     al, 23h
nop
nop

push   ax
```

Lock configuration register

```
pop     ax          ; AL - result
```

➲ ***Write Data to Configuration Register***

For example, write 0FFh to INDEX 3Bh:
Unlock configuration register

```
mov     al, 03bh
out     22h, al
nop
nop
mov     al, 0ffh
out     23h, al
nop
nop
```

Lock configuration register

4.4 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 precedes the transmission, which needs control the TXC signal, and the installing, steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: *Please refer to the section of the "Serial Ports" in the Chapter "System Controllers" for the detail description of the COM port's register.*

➲ ***Initialize COM port***

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: *Control the FB2310 CPU card's DTR signal to the RS-485's TXC communication.*

➲ ***Send out one character (Transmit)***

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

➲ ***Send out one block data (Transmit – the data more than two characters)***

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

➲ ***Receive data***

The RS-485's operation of receiving data is in the same of the RS-232's.

➲ ***Basic Language Example***

a. Initial 86C450 UART

```
10    OPEN "COM1:9600,m,8,1"AS #1 LEN=1
20    REM Reset DTR
30    OUT &H3FC, (INP(%H3FC) AND &HFA)
40    RETURN
```

b. Send out one character to COM1

```
10    REM Enable transmitter by setting DTR ON
20    OUT &H3FC, (INP(&H3FC) OR &H01)
30    REM Send out one character
40    PRINT #1, OUTCHR$
50    REM Check transmitter holding register and shift register
60    IF ((INP(&H3FD) AND &H60) >0) THEN 60
70    REM Disable transmitter by resetting DTR
80    OUT &H3FC, (INP(&H3FC) AND &HEF)
90    RETURN
```

c. Receive one character from COM1

```
10    REM Check COM1: receiver buffer
20    IF LOF(1)<256 THEN 70
30    REM Receiver buffer is empty
40    INPSTR$"
50    RETURN
60    REM Read one character from COM1: buffer
70    INPSTR$=INPUT$(1,#1)
80    RETURN
```

NOTE: The example of the above program is based on COM1 (I/O Address 3F8h). The RS-485 of the PC104-386L uses COM4. If you want to program it, please refer to the BIOS Setup for COM4 address setup.

CHAPTER 5 BIOS SETUP

This chapter describes the PC104-386L BIOS menu displays and explains how to perform common tasks, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit

5.1 BIOS SETUP OVERVIEW

BIOS (Basic Input Output System) is a program used to initialize and set up the I/O devices of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.
After the computer turned on, the BIOS will perform a diagnostics of the system is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

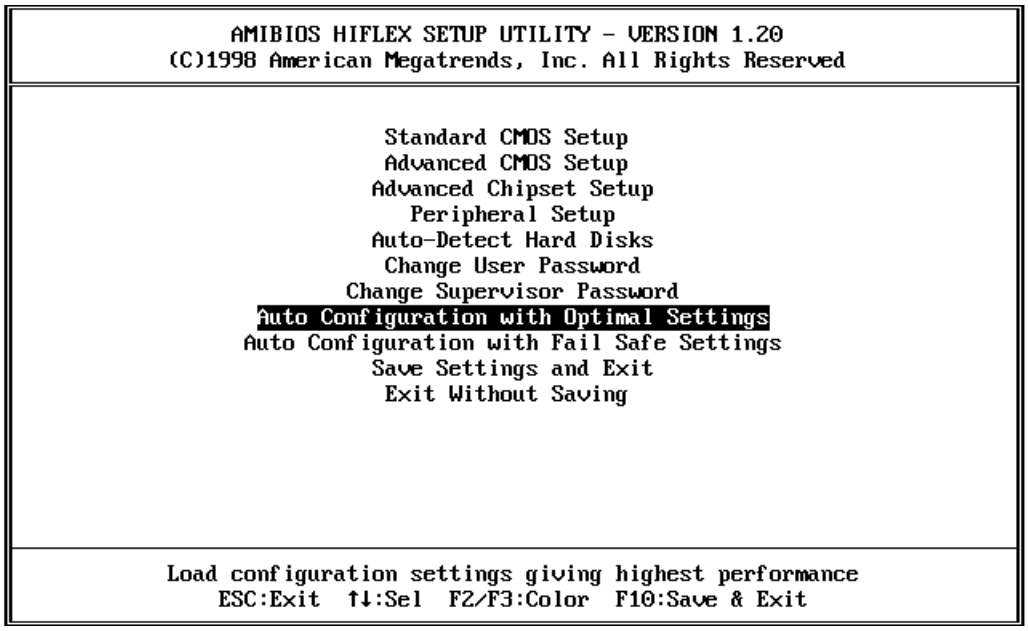

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Change User Password
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving
Load configuration settings giving highest performance
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-1 BIOS Main Menu

CAUTION: 1. The factory-default setting in the FB2310 BIOS is used to the <Auto Configuration with Optimal Settings>, we recommend using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS losses setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. It is recommended to choose the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.

3. The BIOS settings are described in detail in this section.

5.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration, set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

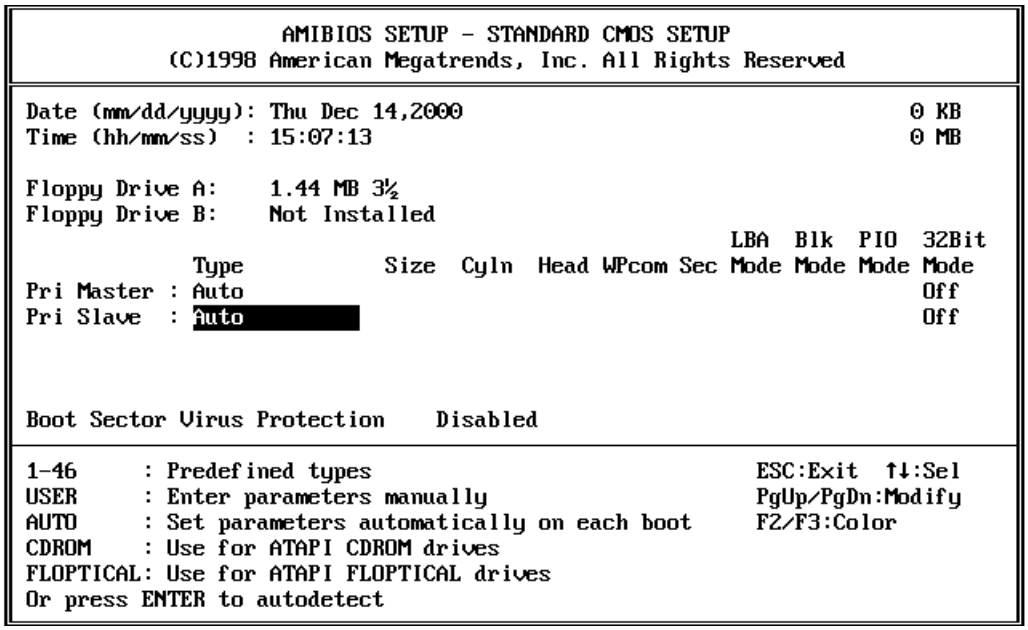

AMIBIOS SETUP - STANDARD CMOS SETUP
(C)1998 American Megatrends, Inc. All Rights Reserved
Date (mm/dd/yyyy): Thu Dec 14,2000
Time (hh/mm/ss) : 15:07:13
0 KB
0 MB
Floppy Drive A: 1.44 MB 3½
Floppy Drive B: Not Installed
Type Size Cyln Head WPcom Sec LBA Mode Blk Mode PIO Mode 32Bit Mode
Pri Master : Auto Off
Pri Slave : Auto Off
Boot Sector Virus Protection Disabled
1-46 : Predefined types
USER : Enter parameters manually
AUTO : Set parameters automatically on each boot
CDROM : Use for ATAPI CDROM drives
FLOPTICAL: Use for ATAPI FLOPTICAL drives
Or press ENTER to autodetect
ESC:Exit ↑↓:Sel
PgUp/PgDn:Modify
F2/F3:Color

Figure 5-2 Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <***Disabled***>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

5.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

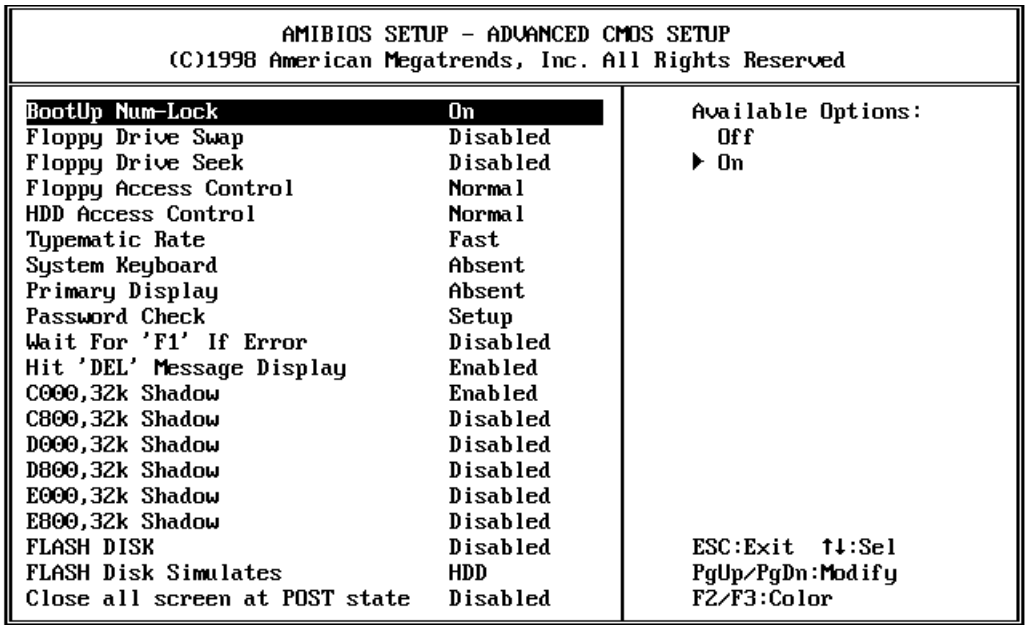


Figure 5-3 Advanced CMOS Setup

1st-3rd Boot Device

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available Options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

S.M.A.R.T for Hard Disks

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available Options: Disabled, Enabled

Default: Disabled

Quick Boot

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.
2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.
3. You can not run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

BootUp Num-Lock

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.
Available Options: On, Off
Default setting: On

Floppy Drive Swap

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is <***Enabled***>, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.
Available Options: Disabled, Enabled
Default setting: Disabled

Floppy Drive Seek

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.
Available Options: Disabled, Enabled
Default setting: Disabled

Floppy Access Control

This field specifies the read/write access when booting from a floppy drive.
Available Options: Normal, Read-only
Default setting: Normal

HDD Access Control

This field specifies the read/write access when booting from a HDD drive.
Available Options: Normal, Read-only
Default setting: Normal

PS/2 Mouse Support

The PS/2 mouse function is optional. Before you configure this field, make sure your FB2310 supports this feature. The setting of ***Enabled*** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.
Available Options: Disabled, Enabled
Default setting: Disabled

Typematic Rate

This function specifies the keystroke repeat rate when a key is pressed and held down.
Available Options: Fast, Slow
Default setting: Fast

System Keyboard

This field specifies if an error message should be prompted when a keyboard is not attached.
Available Options: Absent, Present
Default setting: Absent

Primary Display

The field specifies the type of monitor installed in the system.
Available Options: Absent, Normal

Default setting: Absent

Password Check

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Available Options: Setup, Always

Default setting: Setup

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this field is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available Options: Disabled, Enabled

Default setting: Disabled

Hit 'DEL' Message Display

Set this field to ***Disabled*** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available Options: Disabled, Enabled

Default setting: Enabled

C000, 32k Shadow - E800, 32k shadow

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
3. **Cached**: The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available Options: Disabled, Enabled, And Cached

Default setting: Disabled

FLASH Disk

These fields control the location of the contents of the solid-state disk BIOS beginning at the specified memory location.

Available Options: Disabled, D0000h, D8000, E0000, and E8000

Default setting: Disabled

Flash Disk Simulates

When HDD is selected, the system will boot from the flash disk as if it is a hard disk drive (C). When FDD is selected, the system will boot from the flash disk as if it is a floppy disk drive (a:).

Available Options: HDD, FDD
Default setting: HDD

Close all screen at post

Upon power on, the system will skip POST, and enter the OS in five seconds. If this function is enabled, also configure the following fields to the appointed values.

Hit 'Del' Message Display: Disabled
Wait For 'F1' If Error: Disabled
System Keyboard: Absent
Primary Display: Absent
Hard Disk Display: Disabled

Available Options: Disabled, Enabled
Default setting: Disabled

5.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

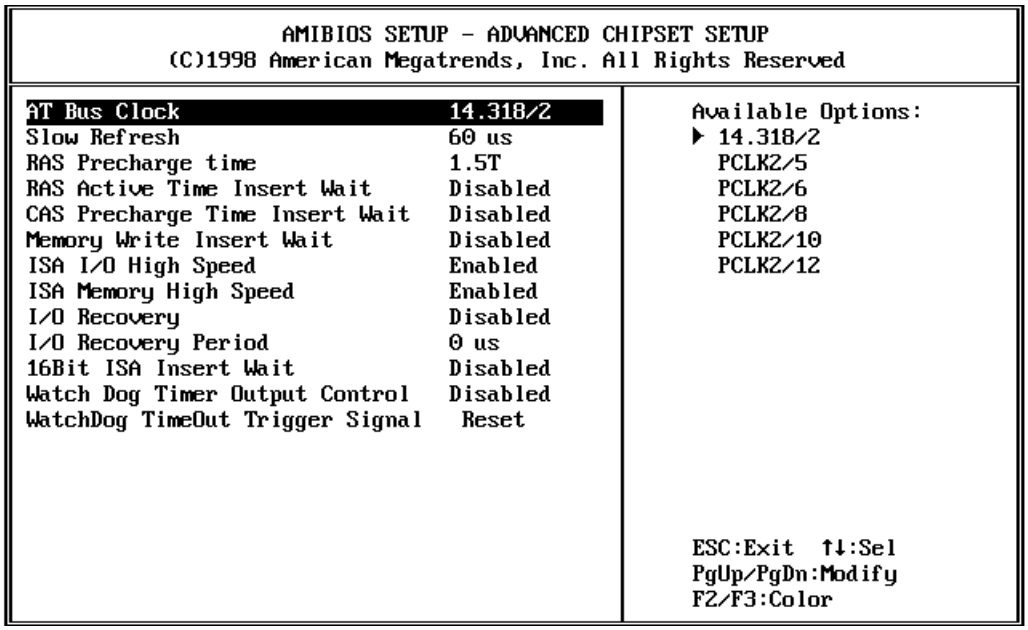


Figure 5-4 Advanced Chipset Setup

AT Bus Clock

This field sets the polling clock speed of ISA Bus (PC/104).
Available Options: 14.318/2, PCLK/5, PCLK/6, PCLK/8, PCLK/12
Default setting: 14.318/2

NOTE: *1. PCLK means the CPU inputs clock.*
2. User is recommended to use setting at the range of 8MHz to 10MHz.

Slow Refresh

This field sets the DRAM refresh cycle time.
Available Options: 15 us, 60 us, and 120 us
Default setting: 60 us

RAS Precharge Time

This field specifies the length of the RAS precharge part of the DRAM access cycle when EDO DRAM is installed.
Available Options: 1.5- 3.5 T
Default setting: 1.5T

RAS Active Time Insert Wait

This field specifies the RAS Active Time Insert Wait function.
Available Options: Disabled, Enabled
Default setting: Disabled

CAS Precharge Time Insert Wait

This field specifies the DRAM CAS precharge time.
Available Options: Disabled, Enabled

Default setting: Disabled

Memory Write Insert Wait

This field specifies the Memory Write Insert Wait function.
Available Options: Disabled, Enabled
Default setting: Disabled

ISA I/O High Speed

The field specifies the ISA I/O High Speed function.
Available Options: Disabled, Enabled
Default setting: Enabled

ISA Memory High Speed

This field specifies the ISA Memory High Speed function
Available Options: Disabled, Enabled
Default setting: Enabled

I/O Recovery

If I/O Recovery Feature field is enabled, the BIOS insert a delay time between two I/O commands. The delay time is defined in I/O Recovery Period field.
Available Options: Disable, Enable
Default setting: Disable

I/O Recovery Period

This specifies the I/O recovery delay time.
Available Options: 0 – 3.5 us
Default setting: 1.5 us

16Bit ISA Insert Wait

This field specifies the 16bit ISA Insert Wait function.
Available Options: Disable, Enable
Default setting: Disable

Watch Dog Timer Output Control

This function is to enable or disable the Watchdog timer function.
Available Options: Disabled, Enabled
Default setting: Disabled

Watch Dog Timeout Trigger Signal

This field can not be configured.

5.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

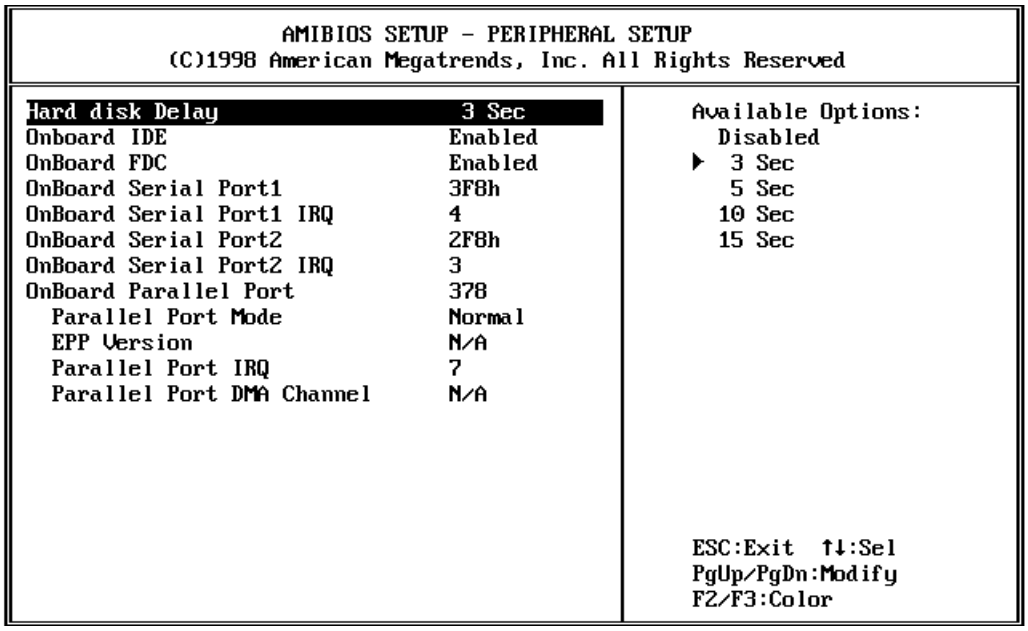


Figure 5-5 Peripheral Setup

Hard Disk Delay

If this field is set to ***Disabled*** and the system BIOS executes too fast, the result is the BIOS can't find the hard disk drive.
Available Options: Disabled, 3 Sec, 5 Sec, 10 Sec, and 15 Sec
Default setting: 3 Sec

OnBoard Primary IDE

This field specifies the onboard primary IDE controller channels that will be used.
Available Options: Disabled, Enabled
Default setting: Enabled

OnBoard FDC

This field enables the floppy drive controller on the FB2310.
Available Options: Disabled, Enabled
Default setting: Enabled

OnBoard Serial Port 1 - 2

These fields select the I/O port address for each Serial port. Refer to Table 2-2.
Available Options: Disabled, 2F8H, 3F8H, 2E8H, 3E8H
Default setting: 3F8H, 2F8H, 3E8H respectively

OnBoard Serial Port 1- 2 IRQ

These fields select the IRQ for each serial port.
Available Options: 3, 4, 5, and 9
Default setting: IRQ4 for Port 1; IRQ3 for Port 2

OnBoard Parallel Port

This field selects the I/O port address for parallel port. Refer to Table 2-2.

Available Options: Auto, Disabled, 378, 278, and 3BCH
Default setting: 378H for Port 1, 278H for Port 2

Parallel Port Mode

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.
Available Options: Normal, EPP, and ECP
Default setting: Normal

EPP Version

This field specifies the EPP for the Parallel Port/Port2 Mode specification version used in the system and is not configurable.

Parallel Port IRQ

This field specifies the IRQ for the parallel port/port 2.
Available Options: 5, 7
Default setting: IRQ7 for Parallel Port; IRQ5 for Parallel Port 2

Parallel Port DMA Channel

These two fields are for monitor only and cannot be configured.

5.6 AUTO-DETECT HARD DISKS

This field detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

5.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

Enter new supervisor password:

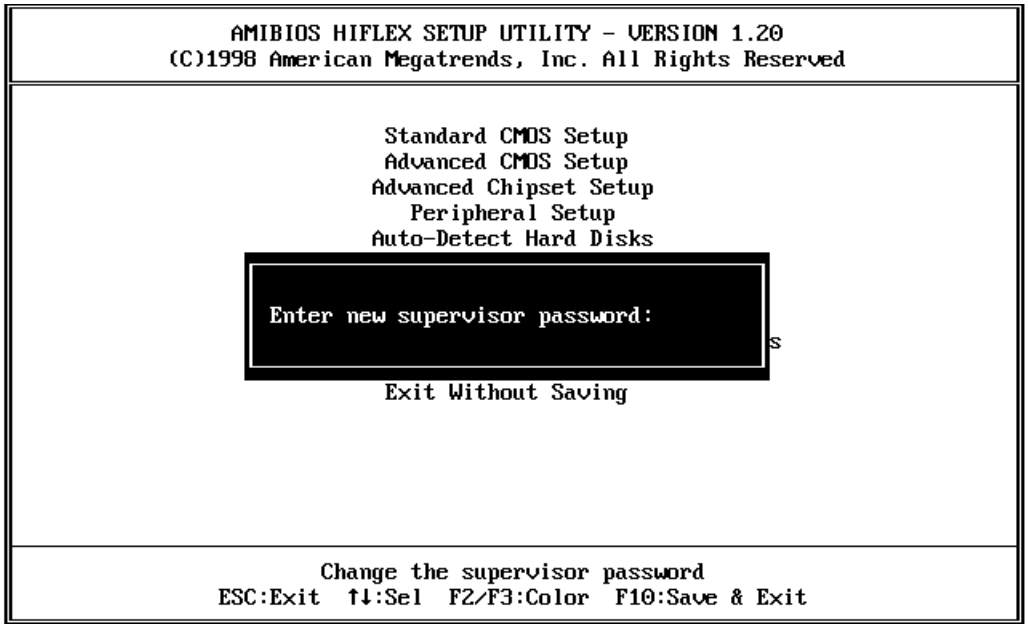

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Enter new supervisor password:
Exit Without Saving
Change the supervisor password
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-6 Enter New Super User Password

Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

5.8 LOAD DEFAULT SETTINGS

It permits user to select a group of setting for all BIOS Setup options. Not only can you use these fields to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

Auto Configuration with Optimal Settings

User can load the optimal default settings for the BIOS. The optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

Load high performance settings (Y/N)?

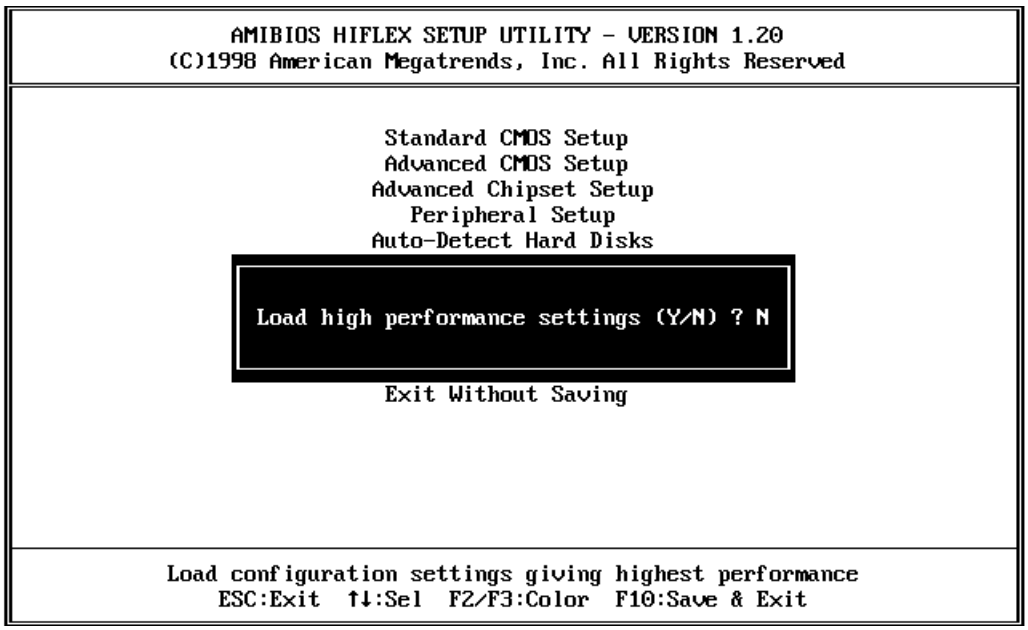

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Load high performance settings (Y/N) ? N
Exit Without Saving
Load configuration settings giving highest performance
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-7 Load High Performance Setting

Auto Configuration with Fail Safe Settings

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

Load failsafe settings (Y/N)?

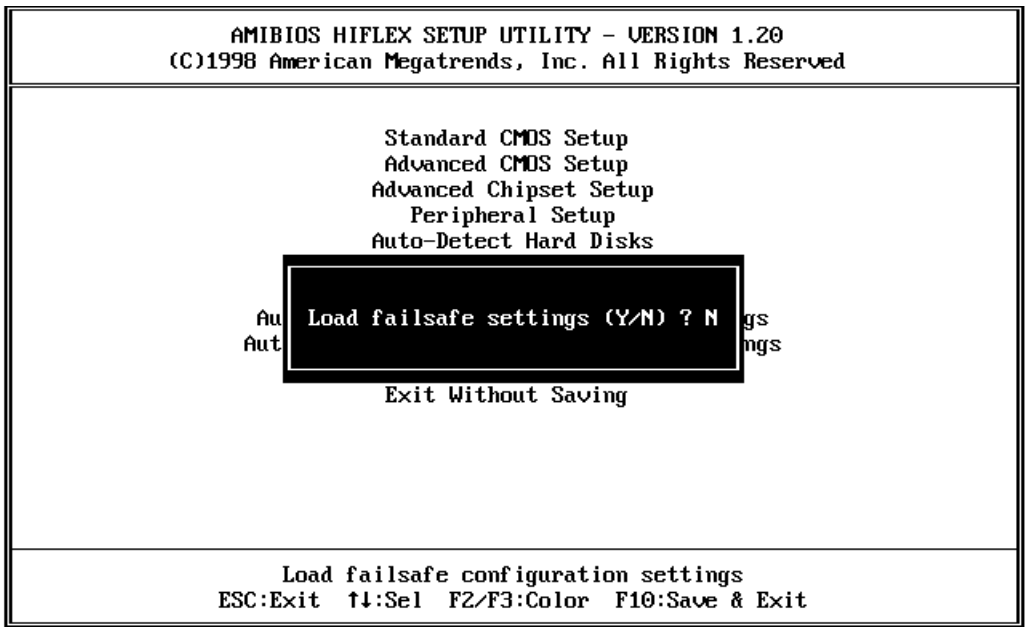

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Load failsafe settings (Y/N) ? N
Exit Without Saving
Load failsafe configuration settings
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-8 Load Failsafe Setting

5.9 BIOS EXIT

It is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

Save Settings and Exit

It is used to save the modified values set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

Save current settings and exit (Y/N)?

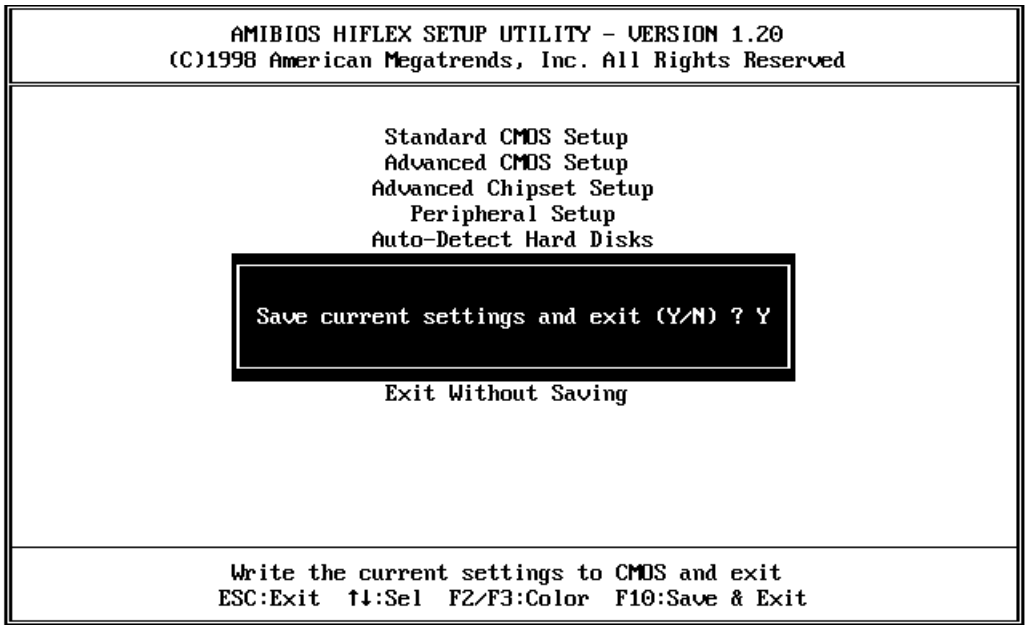

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Save current settings and exit (Y/N) ? Y
Exit Without Saving
Write the current settings to CMOS and exit
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-9 Save Current Settings and Exit

Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to abandon all Data and Exit Setup.

Quit without saving (Y/N)?

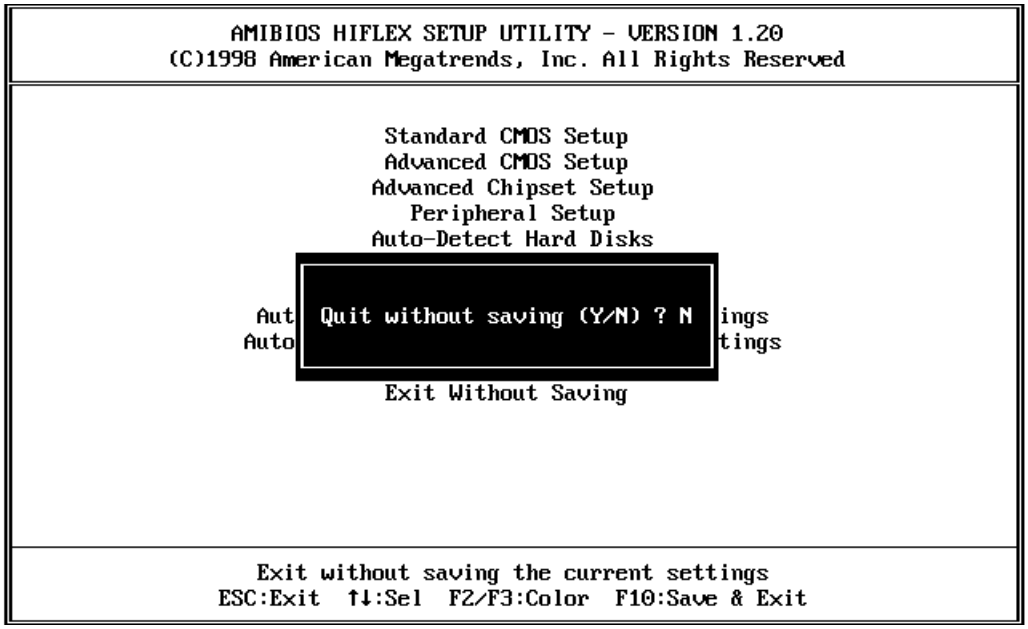

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.20
(C)1998 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Quit without saving (Y/N) ? N
Exit Without Saving
Exit without saving the current settings
ESC:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit

Figure 5-10 Quit Without Saving

5.10 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The FB2310 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Turn on your system and skip detecting the CONFIG.SYS and AUTOEXEC.BAT files. Keep your system in the real mode.

Step 2: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 3: In the MS-DOS mode, you can type the AMIFLASH program.

A:\>AMIFLASH

Step 4: The screen will show the message as follows:

Enter the BIOS File name from which Flash EPROM will be programmed. The File name must and with a <ENTER> or press <ESC> to exit.

Step 5: Enter the file name to the box of <Enter File Name>. And the box of <Message> will show the notice as follows. The bottom of this window always shows the gray statement.

Flash EPROM Programming is going to start. System will not be usable until Programming of Flash EPROM is successfully complete. In case of any error, existing Flash EPROM must be replaced by new program Flash EPROM.

Step 6: As the gray statement, press the <Y> key to updating the new BIOS.
And then the <Message> box will show the <Programming Flash EPROM>, and the gray statement shows <Please Wait>.

Step 7: The BIOS update is successful, the message will show <Flash Update Completed - Pass>.

NOTE: 1. *If the system doesn't detect the boot procedure after power on, please press the [F5] key immediately. The system will pass the CONFIG.SYS and AUTOEXEC.BAT files.*

2. *The BIOS flash disk is not a standard accessory. Now the onboard BIOS are the newest BIOS. If user needs to add some functions in the future, please contact our technical supporting engineers, they will provide the newest BIOS for updating.*

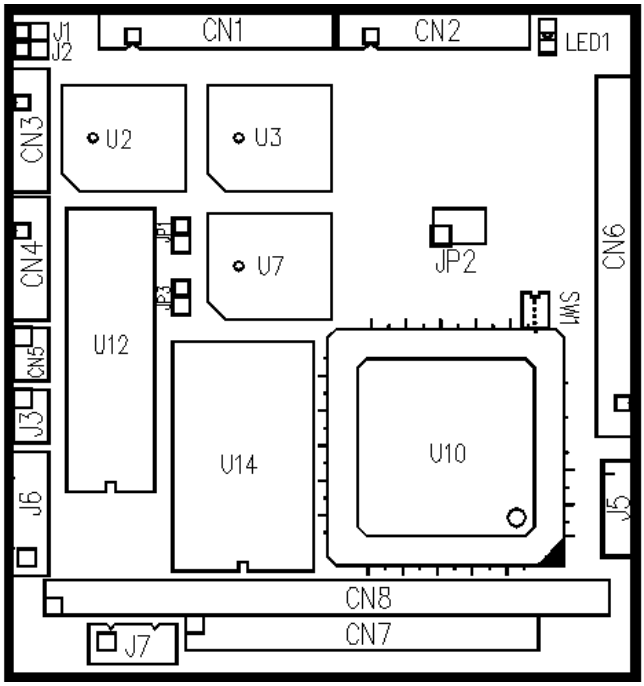
3. *Use the file AMIFLASH.EXE from the attached CD ROM's file. It not, uses Version 6.31.*

APPENDIX

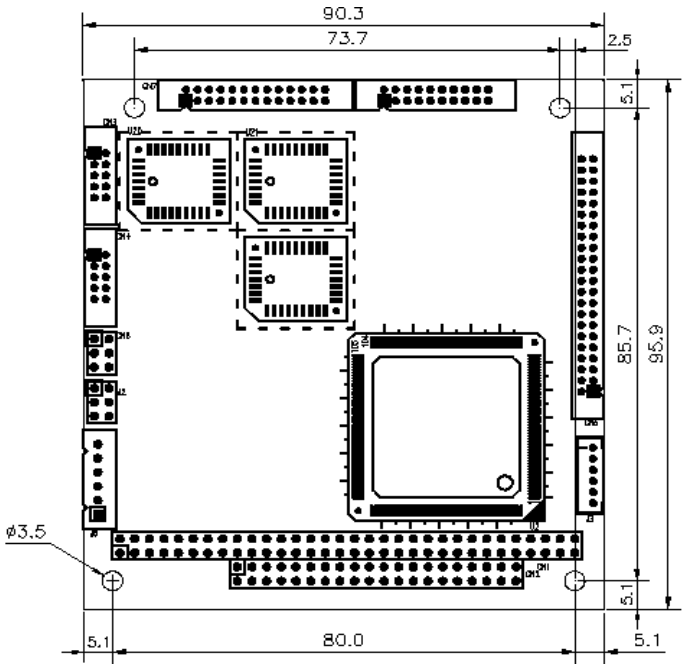
SPECIFICATIONS

CPU & Chipset:	ALI M6117, 33/40 MHz under 5V power supply
Bus Interface:	Stack through PC/104 bus
DRAM:	2MB EDO RAM on-board and 2 MB with 1 socket for expansion
HDC:	Two IDE type hard disk drives
FDC:	Two 5.25" or 3.5" floppy disk drives
Serial Port:	Two full RS-232C ports (RS-485 Option)
Parallel Port:	One bi-directional centronics type parallel port
Keyboard:	PC/AT compatible keyboard with 6-pin mini-din connector
Real Time Clock:	BQ3287MT or compatible chips
BIOS:	Legal AMI Flashed system BIOS
Watchdog:	Programmable Watchdog timer
Solid State Disk:	1.5MB flash disk or 1 socket for up to 288 MB DiskOnChip
Ethernet:	NE2000 compatible
LED Indicator:	Power LED
Power Connector:	One 4-pin and one 8-pin (2.5mm) optional power connector
Power Req.:	+5V, 1.2A maximum
PC Board:	6 layers
Dimensions:	90.2 mmX95.8mm
Form factor:	PC/104 form factor
Safety:	EMI considered on every output signals
Other Optional features:	E2KEY function for safe CMOS data keeping and PS/2 mouse

PLACEMENT


J1
J2
CN1
CN2
LED1
CN3
U2
U3
CN4
JP1
JP3
U7
JP2
CN6
SW1
U12
CN5
J3
U14
U10
J6
J5
CN8
CN7
J7

DIMENSIONS



Unit: mm